IN THE SPECIFICATION

1. Please amend the paragraph starting on page 13, line 2 of the application as follows:

Bus arbitrator 110 comprises inverter 405, AND gate 410, and fast turn-off, slow turn-on controller 420. Controller 420 comprises inverters 421 and [[31]] 431, D-gate flip-flops (FF) 422 and 432, and AND gates 423 and 433. Controller 420 is clocked by the CLOCK signal, which causes D-gate flip-flops 422 and 423 to change state on the falling edges of the CLOCK signal. The inputs to controller 420 are REQ1' and REQ2'. The REQ1' access signal is the same as the REQ1 access request signal and the REQ2' access signal is generated by inverter 405 and AND gate 410. The REQ2' signal lags the REQ1 and REQ2 signals due to the gates delays of inverter 405 and AND gate 410. The respective timing of REQ1, REQ2, REQ1' and REQ2' are shown in FIGURE 5.

2. Please amend the paragraph starting on page 13, line 14 of the application as follows:

AND gate 423 compares the REQ1' access request signal to a time-delayed copy of itself. AND gate 423 sets the EN1 enable signal to Logic 1 only if REQ1' and its time-delayed copy are both equal to Logic 1. The time delay is introduced by D-gate flip-flop 422. However, EN1 returns to Logic 0 as soon as the REQ1' signal goes back to Logic [[1]] 0 (i.e., without waiting for the time-delayed copy from the Q output of D-gate flip-flop 422 to return to Logic [[1]] 0).

3. Please amend the paragraph starting on page 13, line 22 of the application as follows:

Similarly, AND gate 433 compares the REQ2' access request signal to a time-delayed copy of itself. AND gate 433 sets the EN2 enable signal to Logic 1 only if REQ2' and its time-delayed copy are both equal to Logic 1. The time delay is introduced by D-gate flip-flop 432. However, EN2 returns to Logic 0 as soon as the REQ2' signal goes back to Logic [[1]] 0 (i.e., without waiting for the time-delayed copy from the Q output of D-gate flip-flop 432 to return to Logic [[1]] 0).

4. Please amend the paragraph starting on page 15, line 10 of the application as follows:

AND gate 623 compares the REQ1' access request signal to a time-delayed copy of itself. AND gate 623 sets the EN1 enable signal to Logic 1 only if REQ1' and its time-delayed copy are both equal to Logic 1. The time delay is introduced by 2N inverters 622, including inverter 622A, inverter 622B, ..., inverter 622C. However, EN1 returns to Logic 0 as soon as the REQ1' signal goes back to Logic [[1]] 0 (i.e., without waiting for the time-delayed copy from inverters 622 to return to Logic [[1]] 0).

5. Please amend the paragraph starting on page 15, line 18 of the application as follows:

Inverter 605 and AND gate 610 generate the REQ2' access request signal. AND gate 633 compares the [[REQ1']] REQ2' access request signal to a time-delayed copy of itself. AND gate 633 sets the [[EN1]] EN2 enable signal to Logic 1 only if [[REQ1]] REQ2' and its time-delayed copy are both equal to Logic 1. The time delay is introduced by 2N inverters 632, including inverter 632A, inverter 632B, ..., inverter 632C. However, [[EN1]] EN2 returns to Logic 0 as soon as the [[REQ1]] REQ2' signal goes back to Logic [[1]] 0 (i.e., without waiting for the time-delayed copy from inverters 632 to return to Logic [[1]] 0).